(Nick) Jin Sean **Lim**

Doctoral Candidate (Statistics) · Academic Assistant

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Research Interest: Mathematical modeling, simulation and optimization of complex systems.

Work Experience

University of Waikato

Hamilton, New Zealand

Academic Assistant

Feb. 2014 - Present

- Group Tutorials for First Year Mathematics Students
- 1:1 Tutorials by special request from the Disability Office and Scholarship Office
- Assignments and Internal Examination Invigilation and Grading
- Student Ambassador for Community Day in conjunction with the 50th Anniversary for Waikato University

Self Employed

Penang, Malaysia

Pro bono Freelancer

Jun. 2011 - October. 2012

- Microsoft Access Database Management system for Non-Profit Organization
- Independent Web developer and Technical Adviser

Penang Design Centre, Intel

Penang, Malaysia

Design Automation Engineer

May. 2004 - Feb. 2011

Methodology development and maintenance of transistor-level fast SPICE Simulator methodology for complex System-on-chip designs. (2005-2007, 2010)

Methodology and usage development of Fast SPICE simulators.

- Correlation and reconciliation between traditional SPICE and Fast SPICE simulators
- Simulation regression and Automation development for Fast SPICE simulators

Methodology Development and maintenance of transistor-level optimization for Process migration of System-on-Chip design (2007, 2009-2010)

- Methodology and best-known-method development and the go-between for developer and design engineer for transistor level optimization for custom analogue designs.
- Co-develop with CAD developers on strategic capabilities that require immediate turn-around-time
- Co-support and development of schematic migration methodology

Development and maintenance of IBIS (I/O Buffer Information Specification) model generation for signal integrity and noise analysis. (2007-2010)

- Automated parameter extraction of complex drivers according to the IBIS specifications
- Correlation debugging and improvement between transistor simulation and IBIS model in complex full channel simulations
- S-Parameter extraction using Fast Fourier Transform of the drivers' response to a Gaussian pulse stimuli in the time-domain

Development and maintenance of LIBERTY model generation for timing and noise analysis (2009-2010)

- Automated parallel simulations and extraction of the simulations into non-linear table.
- Automated iterative based simulations to determine the timing and load limits of the design
- Correlation debug and model improvement between transistor simulation and LIBERTY model

Execution and methodology development for Logic Verification Regression (2004)

- Register transfer logic versus gate level implementation verification for Microprocessor design
- Utility to detect uninitialized logic states in the gate level implementation

British Telecom Exact, British Telecoms

Cyberjaya, Malaysia

Software Engineering Intern

September. 2003 - December. 2003

- Development of cron based utility for automated patch installation
- Server Side Scripting development of web interface for user self-maintenance and Application push service into mobile phones using OTA download and SOAP services

Education

University of Waikato — *Hamilton, New Zealand*

PhD. in Statistics — *August 2015 - Present*

- Research Topic: Ensemble Learning in High Dimension Datasets
- Supported by University of Waikato Doctoral Scholarship

University of Waikato — *Hamilton, New Zealand*

M.Sc (Research) in Mathematics — *February 2013 - March 2015*

- Research Topic: Star Decompositions of Bipartite Graphs
- Awarded A Zulauf Scholarship for Masters Students.
- Completed with First Class Honours 8.25/9.00 GPA.

Multimedia University — *Cyberjaya, Malaysia*

B.Eng (Electronics) Majoring in Telecommunications — *April 1999 - April 2004*

- Completed with First Class Honours 3.67/4.00 GPA.

Program Committees

New Zealand Mathematics and Statistics Post Graduate Conference — *Taupo, New Zealand*

Organizing Commitee — *November 2015*

- Responsible for on-location support and logistics support and planning for a nation-wide postgraduate conference for 60 students

World Vision, Famine 30 — *Penang, Malaysia*

State-level Organizing Committee — *Aug. 2010*

- Responsible for event and logistics management for a state-level World Vision Famine 30 day.

PDC Intel Work Environment Focus Team — *Penang, Malaysia*

Employee Representative — *2007-2011*

- Responsible for maintaining and improving office environment for 200 employees

PDC Annual Dinner — *Penang, Malaysia*

Organizing Committee — *2008, 2009*

- Responsible for on-location support and logistics support for a department-wide annual dinner for 1000 employees.

PDC PG5.2 "House Warming" — *Penang, Malaysia*

Organizing Committee — *January 2008*

- Responsible for general event management to celebrate the opening of a new office building.

Publications

2015	**J.S. Lim**, Star Decompositions of Bipartite Graphs (Thesis, Master of Science (MSc))	*University of Waikato*
2010	**Neogi, S; Lim, J.S**, Optim Improvements for System on Chip Hard IP designs	*Intel Design Technology and Test Conference*
2009	**Yeoh, K.L.; Lim, J.S.; Goh, K.L.; Tee, S.M.**, Custom digital cell generation flow for 65nm processes	*SoC Design Conference (ISOCC)*
2008	**Tan, F.N; Pang, S.G; Sasidaran, D.;Lee, C.S; Lim, J.S.; Ooi, P.L; Yong, L.K**, Core Excitation Modeling Methodology for Efficient Power Delivery Analysis	*Electronics Packaging Technology Conference*
2007	**Tan, F.N; Chai,Chai, A,; Pang, S.G; Sasidaran, D.; Ng, K.H; Deo, S.C; Lee C.S.; Lim, J.S.; Ooi, P.L; Loke, C.N,; Lim, M.C**, Transient current modeling & power delivery analysis for next gen chipset core	*Electronic Materials and Packaging*
2007	**Chan, P.S; Lim, J.S; M.D Alurkar**, UltraSuite: The complete circuit verification suite	*Intel Design Technology and Test Conference*
2006	**Lim, J.S; Liu, C.F**, Power Estimation Methodology Using Nanosim	*Synopsys User Group Conference*
2006	**Lim, J.S; Chan, P.S; Liu, C.F; Yeoh, K.L**, THOR: The be all and end all of circuit verification central runs	*Intel Design Technology and Test Conference*

Skills

Electronics Engineering	Analog CMOS Design
Electronics Engineering	Transistor Level SPICE simulation
Electronics Engineering	Synopsys .LIB Modelling
Electronics Engineering	IBIS Modelling
Electronics Engineering	Transistor Level Optimization
Electronics Engineering	VLSI and Digital Design
Computer Science	UNIX Shell Scripting
Computer Science	PERL/TCL/LISP Programming
Computer Science	PHP/HTML/Javascript/Jquery/CSS
Computer Science	C/C variants/Java Programming
Computer Science	Database Design
General Skills	LaTeX Typesetting
General Skills	MATLAB simulation
General Skills	Mathematical and Statistical Modelling
General Skills	Mathematical Optimization
General Skills	Machine Learning Algorithms
General Skills	R Statistical Programming
General Skills	Statistical Analysis
Languages	English - Advanced
Languages	Malay - Advanced
Languages	Cantonese - Conversational
Languages	Mandarin - Mandarin
Languages	Southern Min - Native

Honours and Awards

2016-2019	**Recipient**, University of Waikato Doctoral Scholarship	*New Zealand*
2014	**Recipient**, Unviersity of Waikato A Zulauf Scholarship for Masters Students	*New Zealand*
2014	**Honours Society**, University of Waikato Chapter, Golden Keys	*New Zealand*
2004-2010	**Multiple Department and Division Level Awards**, Intel Corporation	*Malaysia*
2004	**Honors Award - Book Prize**, Faculty of Engineering, Multimedia University	*Cyberjaya, Malaysia*
2002	**Runners Up**, Intervarsity Engineering Quiz	*Selangor, Malaysia*